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DESIGN OF A HIGH NOISE IMMUNITY ANALOG FREQUENCY COUNTER

by

Mark Christian Loessel

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DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

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1. INTRODUCTION

This thesis discusses the design of a unique analog frequency counter. Frequency response is not as high as some counters currently on the market, being only 0 to 100 kilohertz. However, the technique used to convert analog input frequency to digital pulses provides more immunity to false triggering than any popular counter of today. The low-cost counter uses state-of-the-art components.

2. DESIGN OBJECTIVES

2.1 Specifications of Currently Produced Counters

The frequency counter was designed expressly for tachometer applications in a factory environment. Shaft speeds are frequently sensed using a magnetic pickup. The output waveform is basically a sinusoid with both amplitude and frequency increasing as shaft speed increases. The amplitude variation is not necessarily proportional to shaft speed variation.

Usually there is considerable electrical noise on any signal in a factory. Brush motors, arc welders, and the 60 hertz standard frequency of ac power all contribute to distortion of the expected sinusoidal waveform. The output waveform of the magnetic speed pickup tends to approach that shown below:

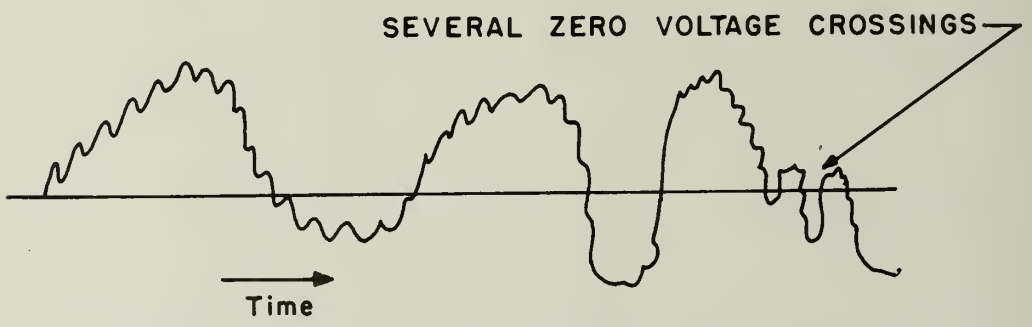


Figure 1. Magnetic Speed Pickup Output Waveform

Many of the commercially available frequency counters, such as Dana, Monsanto, and Tektronix, have only the following operator controls: (1) + pulse, - pulse, or composite; (2) trigger slope, to trigger on leading or trailing edge of waveform; (3) trigger level, 0, +2, -2 volts are the choices if this control is present at all; (4) trigger sensitivity; (5) input attenuation level; and (6) ac or dc coupling.

No combination of settings of these controls can prevent spurious counting of base line voltage crossings as shown in Figure 1. Increasing the trigger sensitivity control will only change the location of the waveform where false triggering will occur. This control determines only the voltage level to be added to the trigger level setting and does not provide hysteresis. Capacitive coupling does little to attenuate the noise especially when the noise frequency approaches the signal frequency. Even adjusting input attenuation such that the noise amplitude is less than the minimum sensitivity of the counter will not work when the input amplitude varies as a function of frequency.

2.2 Advantages of Proposed Counter Design

The proposed method of elimination of noise counts is to incorporate a hysteresis control. The false triggering can then be eliminated by adjusting for more hysteresis than the magnitude of the noise voltage. Purposely limiting bandwidth, in this case to 100 kilohertz, will prevent the counter from seeing fast noise spikes.

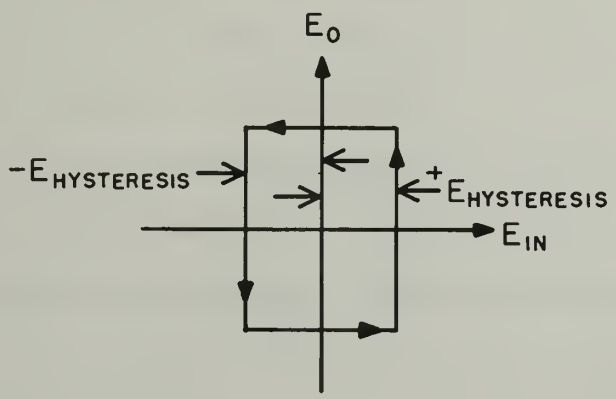


Figure 2. Output Voltage vs. Input Voltage when Hysteresis is Used

By using a variable dc trigger level, one would not have to ac couple any input signal. Input sensitivity could be 50 millivolts rms to match typical

counters. Counter output should be computer compatible for measurement and control of shaft speed. Since an operator has no instantaneous information regarding the data a computer is taking, a numeric display would be desirable. Twenty millisecond response time to .1% full scale accuracy provides a good combination of speed and accuracy. Since input frequency is not high enough to warrant 50 ohm coaxial cable terminations, the input impedance of the counter should be as high as possible to reduce the effects of loading. With the present day trend toward miniaturatization and integration, the counter design should be adaptable, if possible, to LSI (Large Scale Integration) techniques.

Max. Input Frequency. . .	100 kilohertz, 5 microsecond minimum pulse width
Max. Input Voltage. . . .	$\pm$15 volts
Input Impedance	Greater than 100 kilohms
Trigger Level	-15 to +15 volts continuously variable
Trigger Sensitivity . . .	Hysteresis $\pm$50 millivolts to $\pm$500 millivolts
Response Time	Less than 20 milliseconds
Accuracy.	0.1% full scale
Outputs	Digital display, computer compatible
Other Features.	High noise immunity, low cost, design applicable to LSI techniques

Table 1. High Noise Immunity Counter Design Parameters

3. DESIGN OF SENSING CIRCUITRY

3.1 Methods of Implementing a Comparator

There are two basic methods of frequency counting: (1) frequency to analog voltage output, and (2) frequency to digital outputs. In either case, the analog input must first be converted to a digital signal. Many devices are available--bipolar transistors, optical couplers, FET's, and integrated circuit Schmitt triggers and comparators. FET's, especially MOSFET's, would provide very high input impedance. Bipolar transistors probably have the fastest response time. Optical couplers are too slow for the frequency range 0 to 100 kilohertz.

Remembering that the proposed counter should be readily adaptable to LSI methods, it would ease design if one could find a currently produced integrated circuit which, with a few external components, could meet the design requirements. LSI techniques use transistor configurations to replace capacitors, resistors, and diodes. Attempting to breadboard the hundreds of transistors usually found in an LSI package one could easily have reliability or oscillation problems, especially with high gain circuitry. Therefore, the prototype of an LSI design would be very difficult without the help of an IC manufacturer.

Schmitt triggers, comparators, and operational amplifiers are all very high gain circuits available as monolithic IC's. Schmitt triggers that are part of a digital IC logic family have an internally fixed trip level, which would not allow the variable trip level and hysteresis specified in Figure 3.

Advances in recent years have led to new comparator types such as the LM311 [1]. Compared to older industry standards such as Fairchild's μA711, the LM311 is slower (200 ns vs. 40 ns response time), but the LM311 has much better stability and output short circuit protection. A more general purpose integrated circuit is the operational amplifier.

The important specification for selection of an integrated circuit for comparator applications are: (1) gain-bandwidth product to insure minimum specified trigger sensitivity at 100 kilohertz; (2) sufficient output slew rate to allow full output swing at 100 kilohertz; (3) output compatibility with IC logic families; i.e., rise and fall time limitations and ability to source or sink current at the logic voltage levels; (4) input impedance high enough such that the amplifier does not load external component networks; and (5) input voltage range.

Most internally frequency compensated operational amplifiers have a frequency response which approximates a single pole rolloff. This is done because a second order pole response gives 180 degrees of phase shift at unity gain causing positive feedback and subsequent oscillation and destruction of the amplifier [2]. Therefore, dc gain and unity gain crossover frequency are all that are required to completely characterize the frequency response of an internally compensated amplifier.

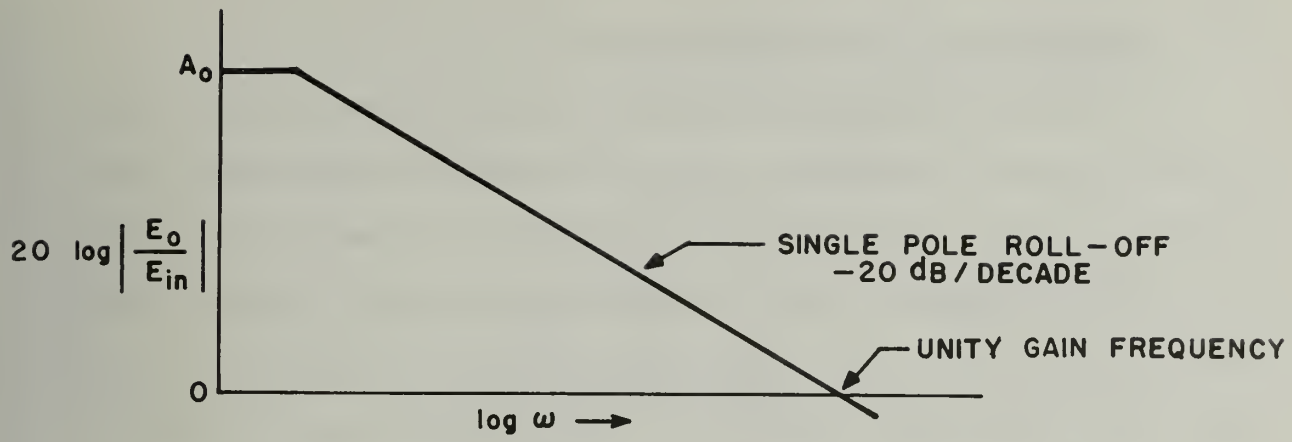


Figure 3. Bode Magnitude Plot for a Typical Internally Compensated Operational Amplifier

Since the logic family to be used could require a high logic level of +10 volts, the gain required at 100 kilohertz is 10 volts divided by the minimum sensitivity of 50 millivolts, or 46 dB. An amplifier with a gain of 46 dB at 100 kilohertz and a single pole rolloff of -20 dB/decade would require a unity-gain crossover frequency of 20 megahertz. For uncompensated amplifiers, usually the unity gain crossover frequency is not specified as this can be greatly varied depending upon the frequency compensation technique used.

For slew rate, assuming $\pm$15 volt swing on output at 100 kilohertz, the minimum slew rate is 3 volts/microsecond. This is slower than the rise time requirement of any IC logic family.

The dc offsets internal to the comparator or amplifier are relatively unimportant as the external dc reference can be used to null the internal offset. Monolithic IC drift, especially for ceramic packages, is better than the drift of the discrete components used in the configuration. Latch-up protection and output short circuit protection are desirable features.

3.2 Data Sheet Search for Usable Devices

After cross-referencing a D.A.T.A. [3] book for specifications and Semiconductor Specialists catalog [4] for pricing and availability, three devices were chosen on the basis of their performance/price ratio: (1) an LM311 comparator, which has high gain, high speed, and high stability when contrasted with other comparators; (2) an LM301A operational amplifier, which is probably the cheapest, most widely second-sourced, moderate performance operational amplifier currently being sold; and (3) the HA2-2625 op amp which has a very high gain-bandwidth product and very high slew rate.

	LM301A	LM311D	HA2-2625
A_0 (gain at dc)	25,000	200,000	80,000
Max V_{in} common mode	±12 v	±15 v	±15 v
Max V_{in} differential	±30 v	±30 v	±30 v
Unity gain bandwidth	---	---	100 MHz
Slew rate	5v/us	200 ns*	20v/us
Cost	75¢/1	$4/1	$8/1
Input Impedance	2 Mohms	---	40 Mohms

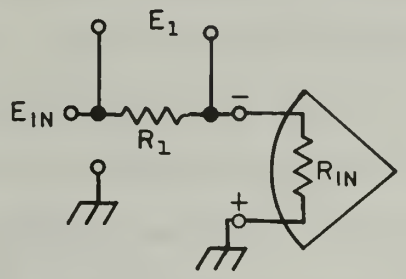
* Comparators usually specify response time.

Table 2. Major Specifications of Selected Devices

3.3 Response of LM301A, LM311D, and HA2-2625

Data sheet parameters are usually only given for a specific set of operation conditions such as R_{in} = 100 ohms, R_{load} = 2 kilohm and power supplies are set at ±15 volts dc. Circuit parameters at other operating conditions must be obtained empirically.

To determine whether input resistance is a function of input voltage level, measurements were conducted as in Figure 4. A Fluke Model 8200A digital voltmeter was used for accuracy.



By resistive divider:

$$R_{in} = \left(\frac{E_{in}}{E_1} - 1\right)R_1$$

Figure 4. Static Input Resistance Measurement

The readings showed that the input resistance increased as the input voltage increased, and I_{in} remained constant. This indicated that the input circuitry is better characterized as an input bias current rather than input resistance. Note that this is a static test only and tells nothing about switching transient effects. For any of the three devices, and for any input voltage in the range of -15 to +15 volts dc, input resistance was at least three megohms.

Frequency response was tested using the configuration of Figure 5. Since the gain of any amplifier rolls off as frequency increases, the point of critical operation will be at 100 kilohertz.

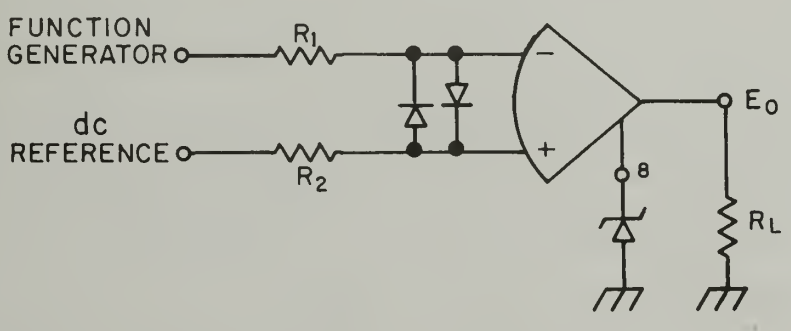


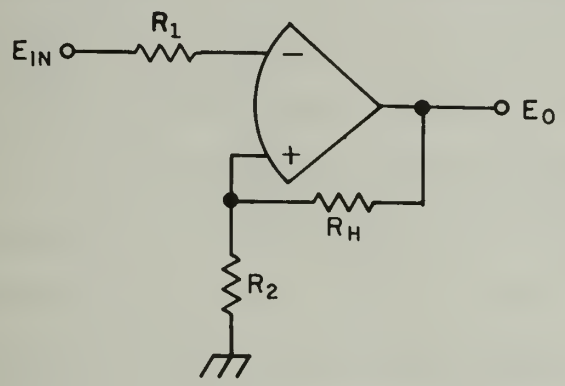
Figure 5. Circuit Used to Measure Gain-Bandwidth Response

All dynamic frequency and voltage measurements were made using a newly calibrated Tektronix Model 434 oscilloscope.

Since the LM301A has no internal frequency compensation, various frequency compensation techniques were tried [5]. Standard compensation of 30 picofarads between terminals 1 and 8 of the mini-DIP package give a slew rate of less than 1 volt per microsecond. This slew rate limits the maximum input frequency for full output swing to less than 15 kilohertz. Feedforward compensation, where the input signal is capacitively coupled to the intermediate stage using 120 picofarads, gives a slew rate of almost 15 volts per microsecond, but the minimum trigger level required for full output swing is $\pm$500 millivolts. Using no frequency compensation, slew rate is almost 30 volts per microsecond and the required minimum trigger level is $\pm$55 millivolts. Therefore, the LM301A was no longer considered because of insufficient gain at 100 kilohertz.

The LM311 was tested, as in Figure 5, to observe the effects of varying external component values. This comparator has internal clamp circuitry such that the output can only swing between zero and positive supply voltage. Using equal input resistors, with the dc reference set at zero volts, it was learned that output slew rate decreases as R_1 and R_2 are increased. For R_1 and R_2 = 100 ohms, response time was .2 microseconds. For R_1 and R_2 equal to 100 kilohms, response time was .4 microseconds. Minimum trigger sensitivity for the two cases increased from $\pm$18 millivolts to $\pm$30 millivolts. Clamp diodes (1N4148's) across the input terminals caused no change that was discernible. Output slew rate also depends upon R_{load} with response time decreasing from .2 microseconds to 2 microseconds as R_{load} increases from 200 ohms to 20 kilohms.

The hysteresis voltage level is determined by the amount of positive feedback, or the amount of output voltage presented to the non-inverting input terminal of the comparator. Since the input resistance of the comparator is high, a resistive divider can be used for feedback as shown in Figure 6.



$$E_H = E^+ = \frac{R_2}{R_2 + R_H}(E_o)$$

Figure 6. Comparator Circuit Using Hysteresis

Since the maximum value of R_1 and R_2 without oscillation was found to be 10 kilohms, and the minimum R_{in} of the comparator was found to be 3 megohms, there should be no interaction. Dynamic switching observation will verify the absence or presence of interaction.

In calculating an expected hysteresis voltage by the formula given in Figure 6, one notes that since the output is internally clamped to swing between zero volts and $+V_{supply}$, and never negative, a negative hysteresis voltage is impossible. This unsymmetric dead zone provided by hysteresis could provide false triggering of the waveform shown in Figure 1. One of the design parameters was to provide as much noise immunity as possible. Subsequently, the LM311 design was abandoned with the hopes that the HA2-2625 could be used successfully.

The HA2-2625, the last of the three selected devices, was also tested for frequency response and gain as in Figure 5. As the HA2-2625 is an operational amplifier, the output swing is approximately centered about zero volts with the output swing maximum being approximately two volts less than the power supply voltages being used. Of four devices ordered for testing, three did not have sufficient slew rate for full output swing at 100 kilohertz, and the fourth's slew rate was 15 volts per microsecond--less than the manufacturer's stated minimum of 20 volts per microsecond. Slew rate and minimum trigger level of $\pm$20 millivolts were independent of R_L provided maximum output current of 18 milliamps was not exceeded. Values of R_1 and R_2 up to 100 kilohms and the use of clamp diodes showed no discernible change.

Since the comparator output should be able to interface to any logic family, various methods of clamping output levels were tried. National Semiconductor recommends using a zener diode from the bandwidth control pin to ground [6]. This point is the high impedance base circuitry of the pnp emitter follower output stage. The addition of the emitter follower diode drop provides output logic levels of zero volts and V_{zener} + .7 volts. If the zener were placed at the output, the logic levels would be V_{zener} and -.7 volts. Connecting the zener diode as shown in Figure 7 utterly destroys frequency response. The reason is that a slow switching zener diode cannot receive enough current from the high impedance connection. Better clamping methods are shown in Figure 7. Now the zener is not required to switch: only low capacitance signal diodes which are much faster. Resistive dividers may be substituted for the zeners provided the resistance of the divider network does not interact with the internal resistance seen at the amplifier terminal. If one were using an operational amplifier which were not latch up protected,

Figure 7 provides a method of keeping the op amp out of saturation and subsequent damage.

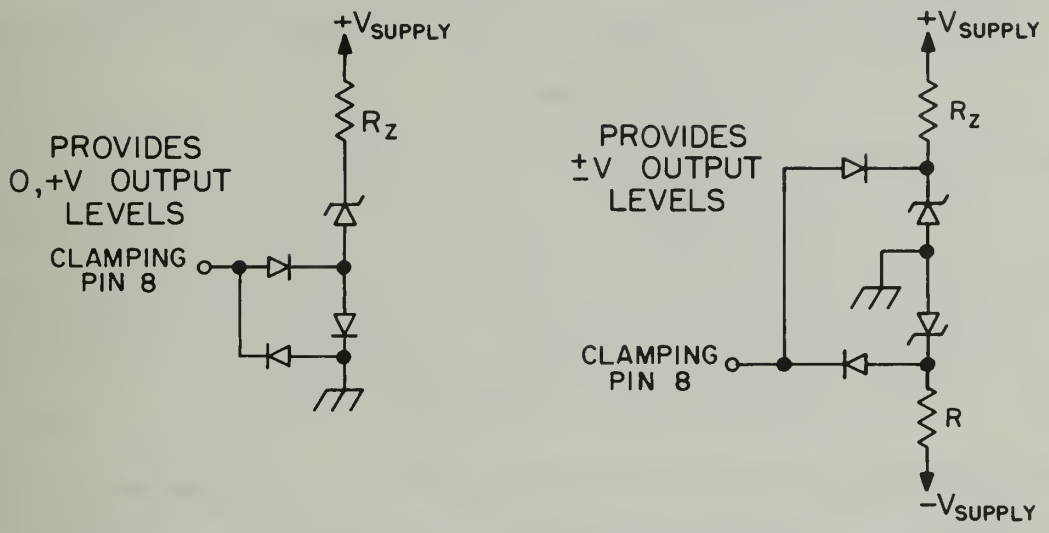


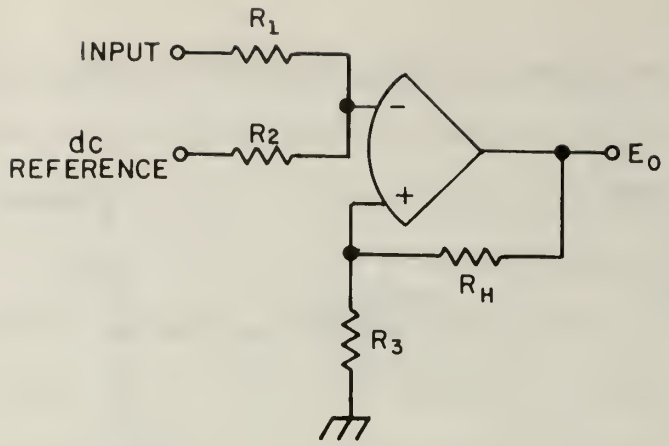
Figure 7. Better Methods of Clamping Comparator Outputs

3.4 Design of Comparator Stage Circuitry

Figure 7 was used to calculate resistor values for various hysteresis levels. For the most general case, when R_2 is not grounded but tied to the dc reference input, the equation for the hysteresis voltage is:

$$E_H = E_{dc\ ref} + (E_0 - E_{dc\ ref}) \frac{R_2}{R_2 + R_H}$$

$E_{dc\ ref}$ is fixed and E_0 is plus or minus depending upon the output state. To eliminate the unsymmetric hysteresis and provide more noise immunity, the configuration shown in Figure 8 should be used.



$$E_H = \frac{R_3}{R_3 + R_H} E_o$$

Figure 8. Comparator Configuration for Symmetric Hysteresis Levels when a dc Reference is Used.

$E_H = E_0 R_3/(R_3+R_H)$, and hysteresis is symmetric and independent of the dc reference setting. The circuit operation is as follows:

$$E_{in} - E_{dc\ ref} < -E_H, \text{ output goes high}$$

$$E_{in} - E_{dc\ ref} > E_H, \text{ output goes low}$$

In all other cases, output stays in past state. Thus, for input levels between $-E_H$ and $+E_H$, no triggering can occur.

Note that in this configuration, assuming $R_1 = R_2$, the input voltage swing is now twice the minimum trigger level required when only the input signal is placed on the inverting input terminal of the operational amplifier. 1% low temperature drift resistors are used for R_1 and R_2 for accuracy.

In selecting resistors R_1, R_2, and R_3, the design trade-off is that large resistor values give higher input impedance while lower resistor values tend to decrease the amount of signal fed back, and minimize the voltage offset due to bias currents. Choose $R_1 = R_2 = 20$ kilohms.

The Thevenin resistance looking out from each amplifier input terminal should be the same to reduce the effect of input offset currents. Therefore, R_3 should equal the parallel combination of R_1 and R_2 or 10 kilohms.

In selecting the value of the hysteresis resistors, the parallel combination of R_3 and R_H should be approximately equal to R_3 to keep the Thevenin resistance the same. As R_H approaches infinity, the hysteresis voltage goes to zero, so there is no upper limit on hysteresis resistance. Discrete values of R_H were chosen rather than a potentiometer to enable one to more easily check if hysteresis levels will change as a function of frequency. Since $E_{0\ max}$ is approximately equal to the supply voltages minus two volts, hysteresis levels are dependent upon supply voltage levels.

E_H:	0	$\pm$25	$\pm$50	$\pm$100	$\pm$250	$\pm$500	millivolts
R_H:		4.7	2.4	1.2	.47	.22	megohms

Table 3. E_H vs. R_H when $E_{0\ max}$ = 12 volts and R_3 = 10 kilohms

Above, E_H does not include inherent minimum trigger sensitivity of the operational amplifier.

Hysteresis voltage increases above that calculated as the upper limit frequency of 100 kilohertz is approached. When observing E_H (the + input terminal of the amplifier), a switching spike shown in Figure 9 was seen. At high frequencies, this spike does not decay fast enough to reach its final value established by the hysteresis level setting. Constructing the circuit on a printed circuit card with ground plane, decoupling the power supply with 47 microfarads in parallel with .01 microfarads located right at the amplifier terminals, did not noticeably

help. This spike must be internal to the amplifier. Possibly reducing all external resistors by an order of magnitude would help. An alternate method is to shunt R_3 with a capacitor. Too little capacitance and the spike is not reduced; too much capacitance and the capacitor will not charge and discharge fast enough to give proper hysteresis levels. The capacitor value of .001 microfarad was optimized empirically with the results shown in Figure 9.

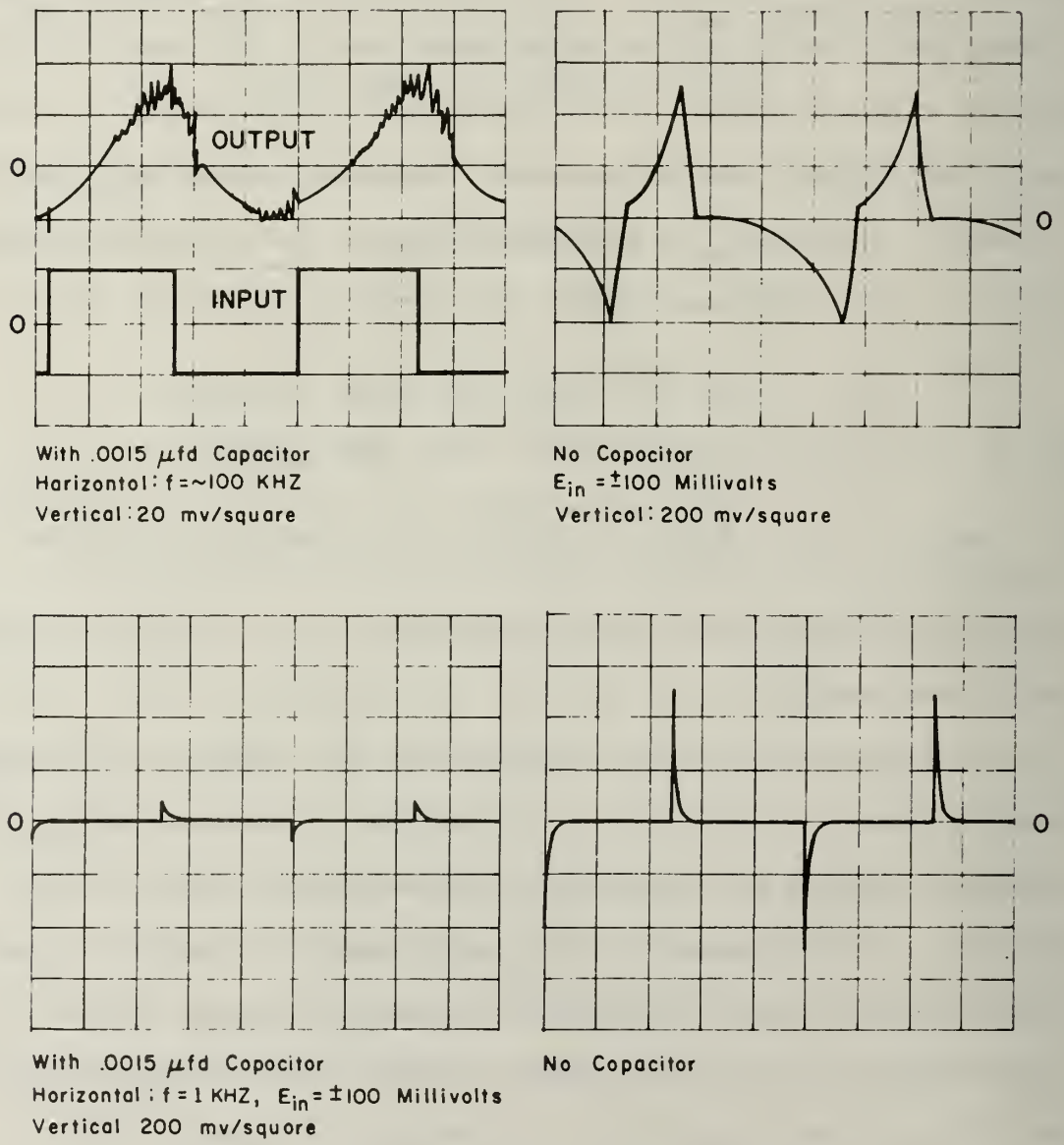


Figure 9. Effect of Capacitance Across R_3 to Eliminate Switching Spike of E_H

Input voltage slew rate affects the minimum trigger sensitivity. Square wave, sinusoid, and triangle, respectively, require more magnitude. This is because the response time of the amplifier requires that the signal be present for a certain time period. In actuality, the fastest pulse the counter will "see" is ±50 millivolts for 3 microseconds. A square wave with essentially no rise time could be only 3 microseconds wide, but a triangular waveform would have to be of either greater magnitude or smaller frequency to meet the requirement. See Figure 10.

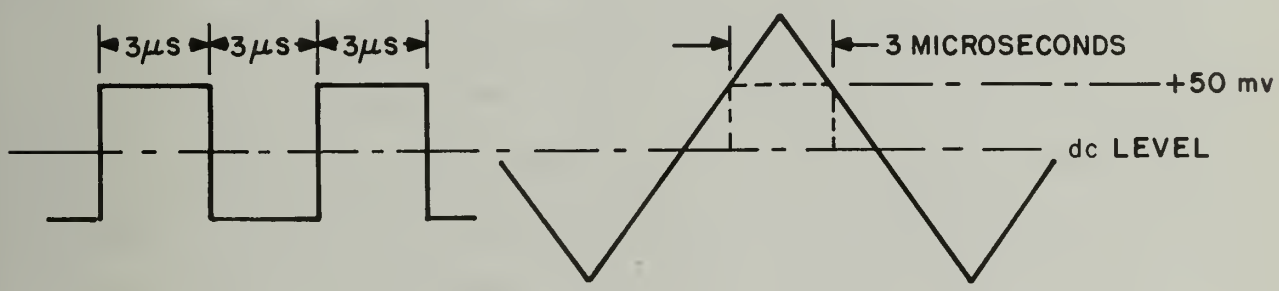


Figure 10. Minimum Trigger Sensitivity Dependence upon Slew Rate of the Input Signal

Approximately 3 to 5 millivolts of dc offset was observed in the switching levels. The manufacturer recommends a resistor between pins 1 and 5, which adds resistance to one of the collector loads of the differential amplifier stage. This is not a good idea for temperature stability. Assuming I_{cbo} doubles for every 10°C. temperature change, the collector voltages would become unbalanced as temperature changes. A better technique would be to incorporate this offset into the dc reference control setting.

For $R_1 = R_2 = 20$ kilohms, the maximum current drawn from the source of the waveform being measured occurs when $(E_{in} - E_{dc\ ref})$ is at the maximum of 30 volts. Then $I_{in} = 30/40$ kilohms = .75 milliamperes, with the sign being either + or -. To increase the impedance of the comparator configuration, an operational amplifier connected as a follower was used. High input impedance, high slew rate, and a flat frequency response to 100 kilohertz are required of the amplifier. The HA2-2625 also works well in this application. The open loop input impedance is 40 megohms, providing 40 megohms input resistance in the follower configuration [7]. If an amplifier were used, the dc level and noise would also be amplified and the hysteresis and dc reference control settings would be harder to figure out. For the lower gain of a follower, the frequency response is more nearly constant for a greater frequency range. The sensitivity requirement has been met without the use of an amplifier.

The dc reference control was buffered using a μA741 in the follower configuration. Gain-bandwidth and slew rate are unimportant for dc applications so the low cost amplifier may be used. This allows a larger resistance potentiometer and, therefore, less current from the power supply without causing interaction with the resistor R_2.

An inverter logic gate on the output of the comparator will provide a choice of $\pm$ trigger slope. Two inverters in series insure that the risetime of the logic signal presented to the counter stage will have the same risetime independent of which trigger slope is selected.

Output level shifting from $\pm E_{0\ max}$ of the comparator to the levels required by the logic family can be accomplished as in Figure 11.

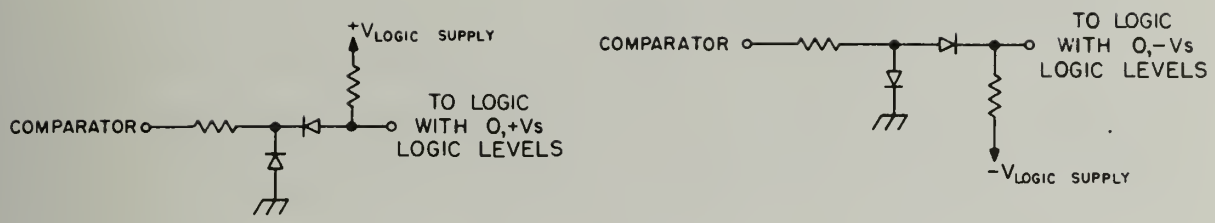


Figure 11. Comparator to Logic Interface

Notice the output swing of the comparator stage was left at its maximum to allow interfacing with any logic family. If one were to choose TTL logic for the counter stage, where the maximum voltage level required is only +3 volts, rather than ±12 volts, only one-fourth the gain is needed, and the LM301A would have sufficient gain. Or, using the gain of the HA2-2625, the minimum input signal required for triggering would be 13 millivolts rather than 50 millivolts. Because E_0 changes, the hysteresis levels would also change.

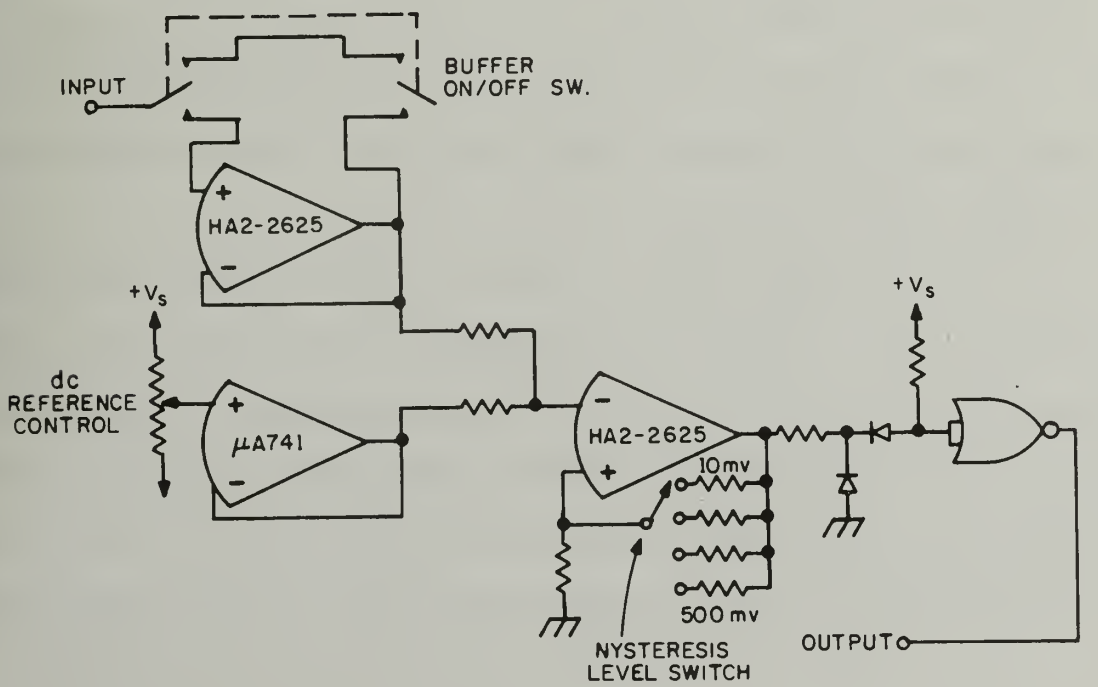


Figure 12. Schematic Diagram of Comparator Stage

4. DESIGN OF DIGITAL CIRCUITRY

4.1 Digital Stage Design Philosophy

The digital section consists of counters, buffers, latches, display, and a clock function to periodically open a time window for counting and closing the window for latch and reset functions.

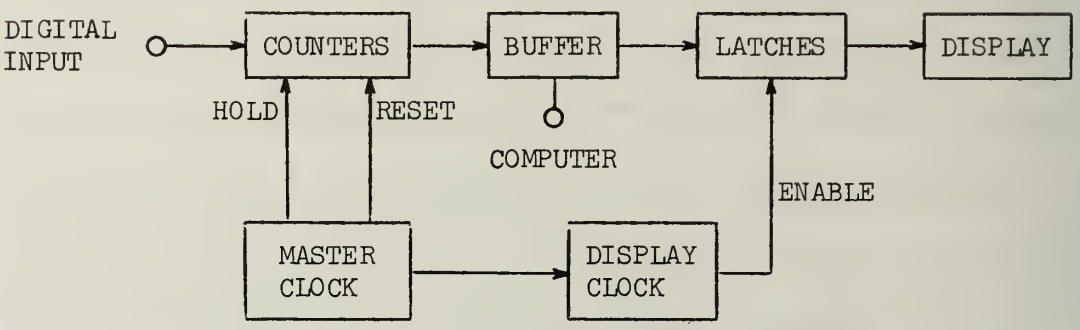


Figure 13. Block Diagram of Digital Section

To determine the type of code to be used as output of the counter stage, remember that 12 bit straight binary or any other code is computer compatible. Software can provide the interpretation. Since the specifications call for a digital display, the counter outputs should be BCD as then BCD to seven-segment decoder/drivers can be used for the display. Other codes do not have the decoder/driver function on a single chip and many packages would be required.

An accuracy of 0.1% full scale and 100 kilohertz full scale input frequency require that the counter be accurate to 100 hertz. The period of the 100 hertz is 10 milliseconds, so the minimum time the counters are enabled is 10 milliseconds. Assuming a square wave clock signal, where the counters are enabled for 10 milliseconds and the latch plus reset time equals 10 milliseconds, the counter response time is the 20 milliseconds specified.

One hundred kilohertz full scale ±.1 kilohertz requires three digits for BCD outputs. BCD counters will be used as then the counters are directly interfaceable to the displays. Hence, there is lower part count, less cost, and greater reliability.

The clocking function must be a highly stable periodic waveform to enable the counters for exactly 10 milliseconds, and provide latch and reset signal while the counters are disabled. Latches will be used to provide a stable display while the counters are enabled. Single shots could be used for the latch enable and reset signals.

The displays should have a separate clock, slower but synchronous with the system clock. Ten millisecond update time provides an update rate of 100 times per second which no human eye can follow if the frequency varied during each clock pulse. A slower rate on the order of five readings per second would be desirable. Since 100 readings per second is not too fast for a computer, the computer enable signal should be left fast to keep the specified response time.

4.2 Selection of Logic Family and Display

The function blocks require decade counters with provision for enable and reset, 4-bit buffers to convert outputs to TTL logic levels if another logic family is used, 4-bit latches for the display, a 3-digit display, a 100 Hertz clock, and single shots.

Before proceeding further, the logic family should be chosen for two reasons: (1) it is possible that some chips, such as the BCD counters are not available in all logic families, and (2) logic ones and zeros may not perform the same function in all logic families, i.e., the counter reset signal required may be a "1" in CMOS and a "0" in TTL.

RTL, DTL, TTL, CMOS, ECL, and high noise immunity logic such as manufactured by Teledyne and Motorola were considered. All of the logic families have the packages needed except for single shots, and they can be made from gates.

In choosing a logic family, one is concerned with speed (maximum clock rate), availability, logic level voltages and current source and sink requirements, noise immunity, power consumption, and compatibility with LSI.

With a maximum input frequency of 100 kilohertz any of the mentioned logic families is fast enough. Voltage levels and current requirements can be taken care of through the design of the interface to the comparator stage. RTL is being phased out by suppliers, all other logic families are readily available.

High speed logic (fast rise time) requires special layout considerations to provide noise immunity. For this reason TTL and ECL will not be considered.

The logic families with the best noise immunity are high noise immunity logic (NHiL), CMOS, and DTL. According to RCA, the noise immunity of their COSMOS is typically one-half the supply voltage.

Considering power requirements, CMOS can be operated from any supply voltage in the range of +3 to +15 volts dc. CMOS power required is a function of frequency, requiring approximately 1 milliwatt at 100 kilohertz. Each TTL low input sources 1.6 milliamperes from a 5 volt supply for 8 milliwatt. CMOS could be operated from the comparator power supply.

With the higher power requirements of TTL, only MSI is possible because of thermal dissipation limitations. This is true for all bipolar

saturated logic. The best logic type for LSI chip density is PMOS, but this is not available in discrete package functions for breadboarding.

Usually, bipolar and MOS semiconductors are not placed on the same chip, so the comparator would have to be on a separate chip. Madhu B. Vora of IBM has recently announced a "BIFET" method for making both MOS and bipolar on the same chip with the same processing steps [8]. If his method proves unfeasible, the logic and comparator could easily be placed on separate chips as there would be few interconnections.

On the basis of the above discussion, CMOS was chosen to implement the logic functions. Price was not used as a determining factor because the newer logic such as CMOS has not yet been produced in great enough volume for the price to bottom out as with TTL, and discrete package costs do not necessarily reflect the cost of a mask for LSI.

When using CMOS, the ideal display would be a liquid crystal display such as RCA's TA8032 because of the low power requirement. At $25 per digit without a decoder driver, the cost was prohibitive.

The display used was Hewlett-Packard's 5082-7300 series display. The latch, decoder-driver, and a .29 character height seven segment display are all integrated into one package. Inputs are BCD and TTL compatible. The TTL levels require power buffering. Texas Instruments make equivalent displays in their TIL306 series, but the cost is higher. As the price of the liquid crystal display falls, the LCD can be used without changing design fundamentals.

4.3 Derivation of Timing Functions

A Signetics NE555 timer module was used for the master clock signal. This low cost (75¢) monolithic chip has a temperature stability of 50 ppm/° C. With only a 3-digit display the accuracy requirements do not warrant the cost of a crystal controlled clock. The output voltage levels of the NE555 depend upon supply voltage and will directly interface to CMOS when operated from the CMOS supply voltage. $\tau_{low} = .685\ R_B C$ and $\tau_{high} = .685\ (R_A + 2\ R_B)C$. From these formulas it is seen that one can never have less than a 50% duty cycle. Using C equal to .01 microfarad, R_B is 15 kilohms and R_A is 1.43 megohms to provide the 10 millisecond and .1 millisecond waveform. A polystyrene capacitor and 1% metal film resistors were used for temperature stability.

The use of a counter with a nonsymmetric duty cycle allows reduction of the time required for latch and reset. Reducing this time to a hundredth of the counter enable time (or .1 milliseconds), the response time is reduced to 10.1 milliseconds. This still allows plenty of time for the latch and counter reset signals.

RCA's CD4000 series of CMOS does not include a single shot package. RCA recommends circuit configurations for both go high and go low single shots using gates [9]. Resistor values must be kept large because of the low source and sink capabilities of a CMOS gate. One disadvantage of using gate configurations for single shots is that both out and $\overline{\text{out}}$ are not available without going through an inverter and increasing package count. Figure 15 shows the poor response time of gates in a single shot configuration.

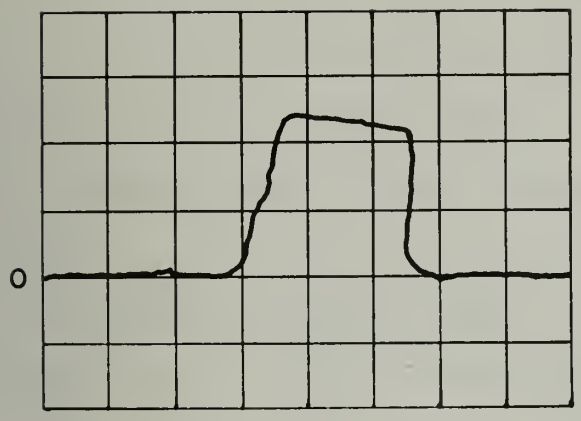


Figure 14. Waveforms Showing Response of Single Shot Made from CMOS Gates

4.4 Digital System Operation

A complete system logic diagram and system timing diagram are shown in Figure 15. The various signals were derived from a configuration which kept package count at a minimum. Except for the buffers, which are only used for compatibility with the TTL inputs of the display, all gates of every package are used.

Both the clock (A) and $\overline{\text{clock}}$ (B) signals are present as (B) is needed for the counter enable signal, but less than a 50% duty cycle is not obtainable from the timer module. The master clock (A) triggers a single shot (C) which is used as a computer latch enable. The pulse width is set to approximately 50 microseconds as this is more easily observable on an oscilloscope.

Counter reset (D) occurs after computer latch (C), but while the counters are still disabled. If a single shot were used to obtain (D),

there is a possibility of a malfunction occurring. The counter could be enabled before the single shot had timed out, causing both reset and enable to be present at the same time. A NAND of (A) and (C) makes sure the counters are enabled when they should be and also allows one NAND gate rather than two for a single shot.

A seven stage binary counter is used to divide down the main clock (A) to obtain a slower update rate for the display. A rotary switch selects one of the seven counter outputs to provide display update rates of 100 to approximately 3/4 hertz. The display counter (E) is triggered on the falling edge of the master clock (A) . A NAND of the computer latch (C) and the display clock (E) insures that the display enable (F) is synchronized with the computer latch enable.

A second single shot (H) is used to insure that the display counter reset signal is present for the minimum reset pulse width of 600 nanoseconds.

The decade counters were connected as parallel counters to insure that the outputs would all change synchronously. In the ripple count mode, the carry must propogate through the counter outputs one by one, causing an error if the disable signal occurs before the final status of each bit has been determined.

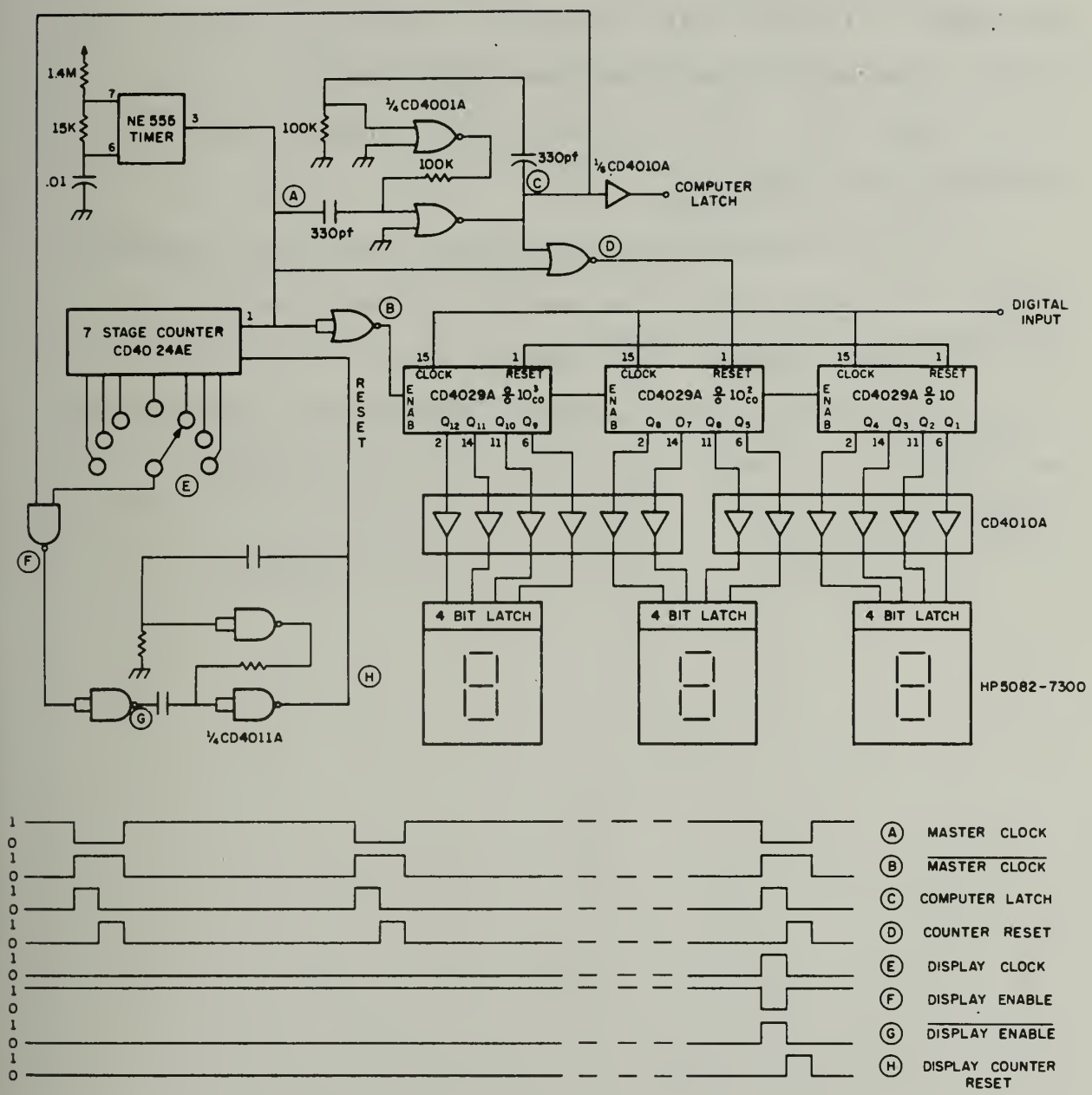


Figure 15. Logic and Timing Diagrams for Digital Section

5. SUMMARY

This thesis discusses the design of a unique analog or digital frequency counter. An accurate count is obtained even when large magnitudes of electrical noise are present. The sensing technique used is an IC comparator with variable threshold and hysteresis settings. A noise immunity of 7.5 volts is obtained in the digital circuitry through the use of CMOS logic.

A 0 to 100 kilohertz $\pm$.1% counter was constructed using this design. The counter uses low cost monolithic circuits and could be built on a single chip using LSI techniques.

The counter was tested using a 6-digit counter and oscilloscope for comparison. All design specifications were met or exceeded.

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APPENDIX A

SYSTEM PACKAGING

The counter system prototype is shown in Figures 16 and 17. The system was constructed on printed circuit cards to eliminate broken wire problems and minimize logic signal interactions. The packaging method shown incorporated materials on hand and is not intended as an optimum packaging design for production.

Three cards were used: (1) comparator, (2) clock and counter, and (3) display and associated circuitry. Card 3 may be eliminated if only computer interfacing is required. Card 2 may be eliminated if a computer is available for timing and counting and only the comparator stage is required.

The entire circuit could be constructed on one printed circuit card 3-1/2" x 9" with all switches and potentiometers mounted on the PC board. A one card system reduces interconnections and corresponding assembly labor.

The ultimate in packaging would be to put the whole system on one or two LSI chips.

The present comparator design requires an external power supply providing 50 milliamperes at $\pm$ 15 volts and 550 milliamperes at +5 volts. The comparator operational amplifier has a power supply rejection ratio of 90 dB, enabling one to calculate the ripple and requlation requirements of the power supply.

Figure A-1. Packaged Prototype of Counter System

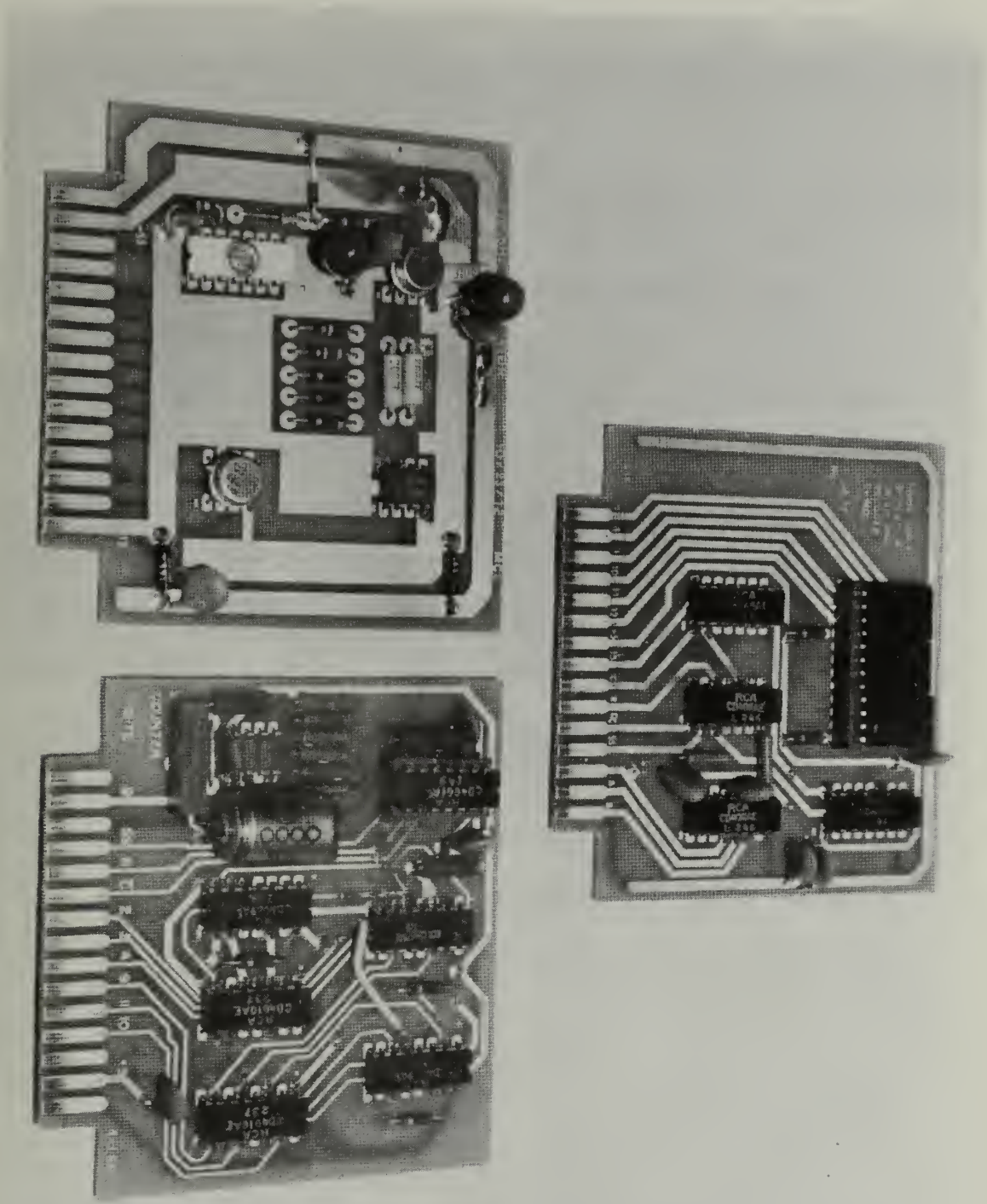

Figure A-2. Circuit Board Layouts

APPENDIX B

OPERATING INSTRUCTIONS

The operator controls are as follows: INPUT BUFFER ON/OFF, DC REFERENCE, DISPLAY REP RATE, and HYSTERESIS.

INPUT BUFFER ON/OFF allows the user to select an input impedance of 40 megohms in the ON position. In the OFF position, the maximum current drawn in .75 milliampere. The ON position buffer provides a fixed slew rate to the comparator of 20 volts/microsecond, and therefore decreases effective risetime of the input waveform. This is noticeable only for square wave input.

DC REFERENCE should be set at the ac midpoint of the input waveform. If the control is not set on the midpoint, the capacitor from the non-inverting input to ground does not charge and discharge at the same rate resulting in unbalanced hysteresis levels.

DISPLAY REP RATE allows the user to select 3/4 to 100 display changes per second.

HYSTERESIS should be set for a value less than the input signal amplitude of the waveform to be measured but greater than the maximum expected noise pulse.

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15. Supplementary Notes

16. Abstracts

This thesis discusses the design of a unique analog frequency counter. Frequency response is not as high as some counters currently on the market, being only 0 to 100 kilohertz. However, the technique used to convert analog input frequency to digital pulses provides more immunity to false triggering than any popular counter of today. The low-cost counter uses state-of-the-art components.

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analog frequency counter
digital pulses

17b. Identifiers/Open-Ended Terms

17c. COSATI Field/Group

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